MM58174 Microprocessor-Compatible Real-Time Clock

General Description

The MM58174 is a low threshold metal gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Time-keeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768 Hz crystal controlled oscillator.

- Independent interrupt system with free drain output
- TTL compatible
- Low power standby operation (2.2V, 10 μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package

Features

- Microprocessor-compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Fast access time (500 ns)

Applications

- Point of sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

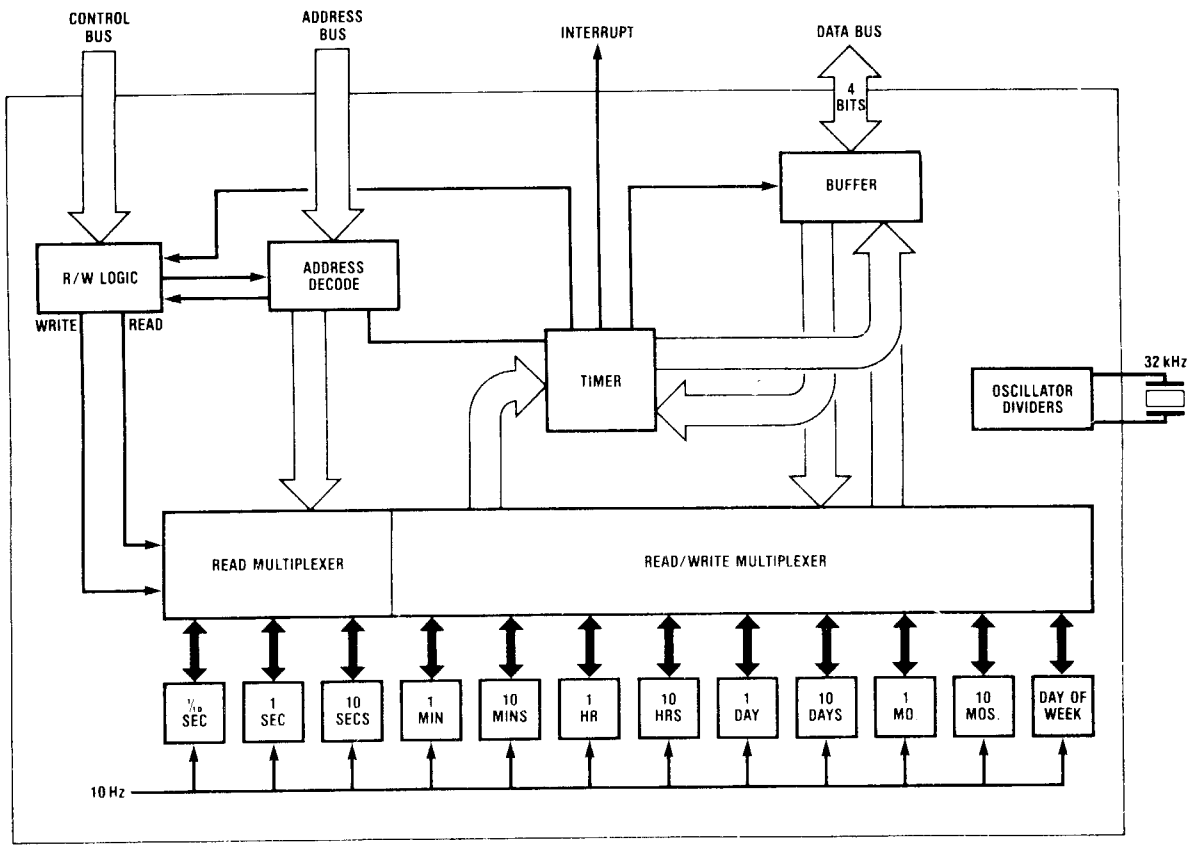


Figure 1. Block Diagram

Absolute Maximum Ratings

Voltage at All Inputs and Outputs	$V_{DD} + 0.3$ to $V_{SS} - 0.3$
Operating Temperature	0 °C to 70 °C
Storage Temperature	−65 °C to +150 °C
$V_{DD} - V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300 °C

Electrical Characteristics $T_A = 0$ °C to +70 °C, $V_{SS} = 0$V

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, V_{DD}	Stand-by mode (no READ or WRITE instructions)	2.2			V
Supply Current, I_{DD}	Operational mode	4.0		6.0	V
	$V_{DD} = 2.5$V		4.0	10	μA
	$V_{DD} = 5.0$V		1.0		mA
Input Logic Levels	$V_{DD} = 5.0$V				
for signals: AD_0-AD_3, DB_0-DB_3, NWDS, NRDS, $\overline{CS}$					
Logic "1"		2.0			V
Logic "0"				0.8	V
Input Capacitance				10	pF
Input Current Levels	$V_{DD} = 5.0$V				
Current to V_{SS} for signals: AD_0-AD_3, DB_0-DB_3, NRDS	$V_{IN} = V_{DD}$			20	μA
Internal Resistor to V_{DD} for signals:					
NWDS		50	100		kΩ
$\overline{CS}$		10	100		kΩ
Output Logic Levels	$V_{DD} = 5$V				
for signals: DB_0-DB_3					
Logic "1"	$I_{OH} = 0.1$ mA	2.4			V
Logic "0"	$I_{OL} = 1.6$ mA			0.4	V
INTERRUPT					
Logic "0"	For $I_{DS} = 5$ mA			1.0	V
Off Leakage	$V_{OUT} = 5$V			5	μA

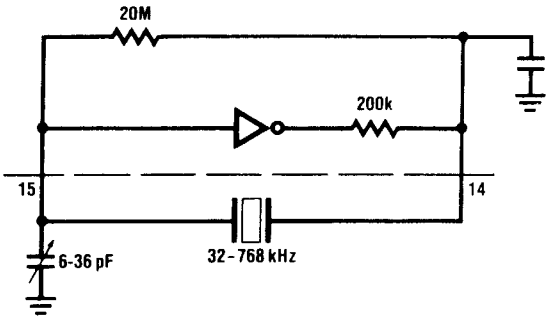


Figure 2. Crystal Oscillator

Days Counter

There are two Days Counters:

a) units of days

b) tens of days

The Days counters will count up to 28, 29, 30, or 31 days depending on the state of the Months counters and the Years Status Register. Days counters have parallel load and read multiplex capabilities.

Months Counters

There are two Months counters:

a) units of months

b) tens of months

The Months counters have parallel load and read multiplex capabilities.

Years Status Register

The Years Status register is a shift register of 4 bits. It will be shifted every year on December 31st. The status register must be set in accordance with Table 3. No readout capability is provided.

Chip Select (CS)

An external chip select is provided. The chip enable is active low.

Counter and Register Selection

Table 1 shows the coding on the address lines AD_0-AD_3 which select the registers in the circuit to be either parallel loaded or read on to the output bus.

Interrupt Output

An exclusive address selects the interrupt latches (address 15). These latches enable the interrupt output and dictate the frequency of the interrupt as shown in Table 2. The interrupt output flip flop is reset by reading the interrupt register. Writing DB_3 at chip address 15 (F) selects single or repeated interrupt.

The contents of the interrupt register are read onto the data bus by reading the interrupt status of the circuit. Table 2 gives the interrupt bits corresponding to data bus bits. DB_3 indicates that an interrupt has occurred. The trailing edge of the NRDS pulse that reads the interrupt status automatically reset DB_3 to zero. The next

Table 1. Address Decoding for Internal Registers

Selected Counter	Address Bits AD_3	AD_2	AD_1	AD_1	Mode
0 Test Only	0	0	0	0	Write only
1 Tenths of secs.	0	0	0	1	Read only
2 Units of secs.	0	0	1	0	Read only
3 Tens of secs.	0	0	1	1	Read only
4 Units of mins.	0	1	0	0	Read or Write
5 Tens of mins.	0	1	0	1	Read or Write
6 Units of hours	0	1	1	0	Read or Write
7 Tens of hours	0	1	1	1	Read or Write
8 Units of days	1	0	0	0	Read or Write
9 Tens of days	1	0	0	1	Read or Write
10 Day of week	1	0	1	0	Read or Write
11 Units of months	1	0	1	1	Read or Write
12 Tens of months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write Only
14 Stop/Start	1	1	1	0	Write Only
15 Interrupt & Status	1	1	1	1	Read or Write

Table 2a. Interrupt Selection Data

Mode: Address 15, Write Mode				
Function	**DB_3**	**DB_2**	**DB_1**	**DB_0**
No Interrrupt	X	0	0	0
Int. at 6.0 sec. intervals*	0/1	1	0	0
Int. at 5.0 sec. intervals*	0/1	0	1	0
Int. at 0.5 sec. intervals*	0/1	0	0	1

* ±16.6ms

$DB_3 = 0$, single interrupt $DB_3 = 1$, repeated interrupt

Table 2b. Interrupt Read Back (Status)

Mode: Address 15, Read Mode				
Interrupt Status	**DB_3**	**DB_2**	**DB_1**	**DB_0**
Reset	0	0	0	0
60 sec. signal	0/1	1	0	0
5.0 sec. signal	0/1	0	1	0
0.5 sec. signal	0/1	0	0	1

$DB_3 = 0$, no interrupt $DB_3 = 1$, interrupt from timer

Table 3 Years Status Register

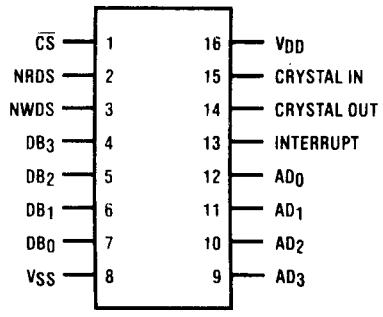
Mode: Address 13, Write Mode				
	DB_3	**DB_2**	**DB_1**	**DB_0**
Leap year	1	0	0	0
Leap year + 1	0	1	0	0
Leap year + 1	0	0	1	0
Leap year + 1	0	0	0	1

Functional Description

The MM58174 is a microprocessor bus-oriented real-time clock. The circuit includes addressable real-time counters for tenths of seconds through months and a write only register for leap year calculation. The counters are arranged as bytes of four bits each. When addressed a byte will appear on the data I/O bus so that each word can be accessed independently. If any byte does not contain four bits (e.g. days of the week uses only 3 bits), the unused bits will be unrecognized during a write operation and tied to V_{SS} during a read operation.

The addressable reset latch causes the pre-scaler, tenths of seconds, seconds, and tens of seconds to be held in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code '1111'. The interrupt timer may be programmed for intervals of 0.5 second, 5 seconds, or 60 seconds and may be coded as a single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the status and internal selected information.

Connection Diagram



Order Number MM58174N
See Package 19

Circuit Description

The block diagram shown in Figure 1 shows the structure of the CMOS clock chip. A 16-pin DIL package is used.

Crystal Oscillator

This consists of a CMOS inverter/amplifier with on-chip bias resistor and capacitors. A single 6-36 pF trimmer is all that is required to fine tune the crystal (see Figure 2). The output of the oscillator is blocked by the start/stop F/F.

Non-Integer Divider

This counter divides the incoming 32,768 Hz frequency by 15/16 down to 30,720 Hz.

Fixed Divider (512)

This is a standard 9 stage binary ripple counter. Output frequency is 60 Hz. This counter is reset to zero by start/stop F/F.

Fixed Divider (6)

This is a three stage Johnson counter with a 10 Hz output signal. This counter is reset to zero state by the start/stop F/F.

Synchronization Stage

Both 10 Hz and 32,768 Hz clocks are fed into this section. It is used to generate a pulse of 15.25 s width on the rising edge of each 10 Hz pulse.

This pulse is used to increment all the seconds, minutes, hours, days, months, and year counter and also to set the data changed F/F.

Data Changed F/F

This is set by the rising edge of each 10 Hz pulse to indicate that the clock value has changed since the last read operation. It is reset by any clock read command. The flip flop sets all data bus bits to a "1" during NRDS time indicating that a register has been updated.

Seconds Counters

There are three counters for the seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds

The outputs of all three counters can be separately multiplexed on to the command 4-bit output bus. Table 1 shows the address decoding for each counter. All three counters are reset to zero by the start/stop F/F.

Minutes Counters

There are two Minutes counters:

a) units of minutes

b) tens of minutes

Both counters are parallel loaded with data from the 4-bit input bus when addressed by the microprocessor and a Write Data Strobe pulse given. Similarly, the output of both counters can be read separately onto the common 4-bit output bus (Table 1).

Hours Counters

There are two Hours counters which will count in a 24 hour mode:

a) units of hours

b) tens of hours

Both counters have identical parallel load and read multiplex features to the Minutes counters.

Seven Day Counter

There is a seven state counter wnich increments every 24 hours. It will have identical parallel load and read multiplex capabilities to the Minutes and Hours counters. The counter counts cyclically from 1-7.

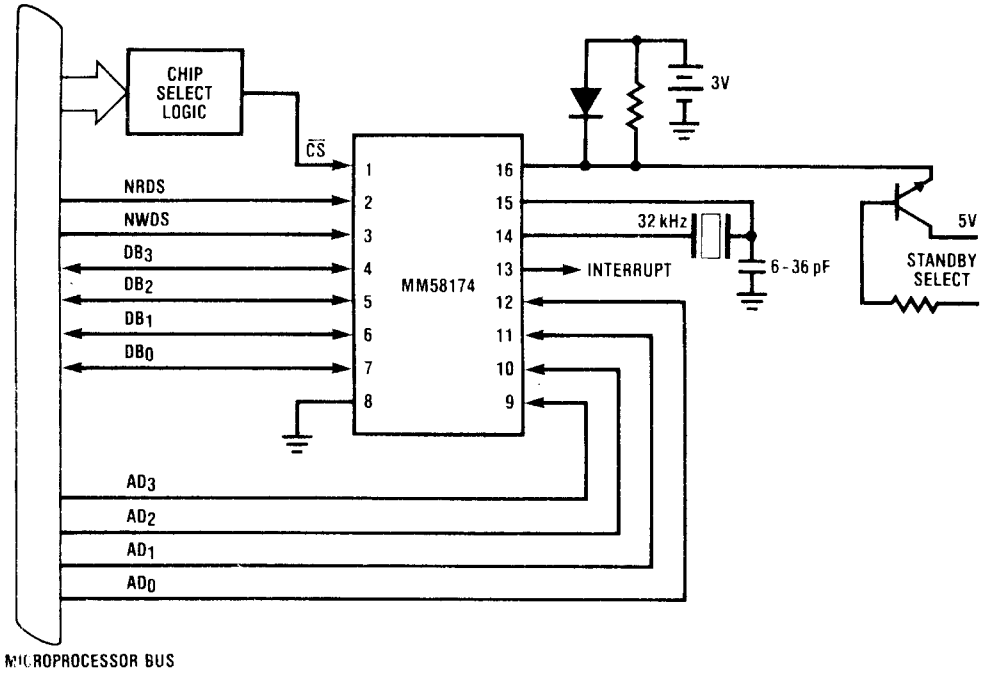


Figure 4. Typical Microprocessor Interface

Timing Waveforms

Read Mode

Figure 5 gives detailed timing in accordance with the Microbus Specification for Microprocessors for the transfer of data from peripheral to microprocessor. See Table 4.

All times are measured from (or to) valid logic "0" level = 0.8V or valid logic "1" level = 2.0V.

Write Mode

Figure 6 gives detailed timing in accordance with the Microbus Specification for Microprocessors for the transfer of data from Microprocessor to peripheral. See Table 5.

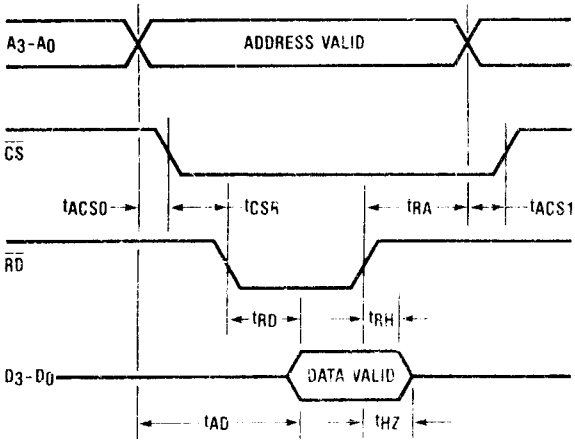


Figure 5. Read Cycle Waveforms

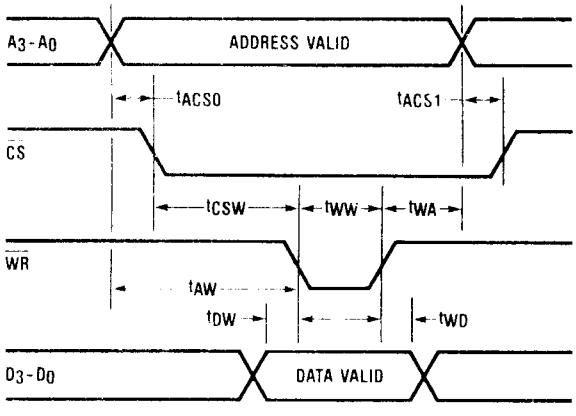


Figure 6. Write Cycle Waveforms

system NRDS pulse after that which has read the interrupt status automatically restarts the interrupt timer if in continuous mode.

When DB_3 is set to zero at chip address 15 (F) the timer is reset at the completion of the selected timing period and must be set by software if a subsequent interrupt is required. Setting DB_3 to 1 allows automatic repeated timer interrupts, starting after the next system NRDS pulse after that which has read the interrupt register.

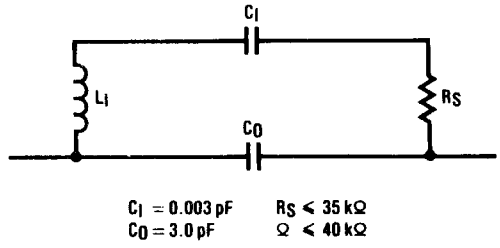
Interrupt should be initialized by applying the reset condition and reading three times at address 15 (F).

Start/Stop

A logic "1" on DB_0 at chip address 14 (E) will start the clock running, a logic "0" will stop the clock. This function allows the loading of time data into the clock and its precise starting.

Test Mode

This mode is incorporated to facilitate production testing of the circuit. For normal operation, the circuit must be set to the non-test mode as part of the system initialization. This is accomplished by writing a logic "0" to DB_3 at AD_0.



$C_I = 0.003\,pF$ $R_S < 35\,k\Omega$
$C_O = 3.0\,pF$ $Q < 40\,k\Omega$

Figure 3. Typical Crystal Parameters

Table 4. Timing: Data from Peripheral to Microprocessor

Symbol	Parameter	Min.	Typ.	Max.	Units	Comm.
t_{ACS0}	Address. Bus Valid to Chip Select ON (CS = 0)		40		ns	$V_{DD} = 5V$
t_{CSR}	Chip Select ON to Read Strobe	70			ns	
t_{RD}	Read Cycle Access Time from Read Strobe to Data Bus Valid		450	500	ns	CL = 100 pF
t_{RH}	Data hold time from trailing edge of Read Stobe	0		250	ns	
t_{RA}	Address Bus hold time from trailing edge of Read Strobe	50	500		ns	
t_{ACS1}	Address change to Chip Select OFF		40		ns	
t_{AD}	Address Bus Valid to Data Valid		850	1200	ns	CL = 100 pF
t_{HZ}	Time from trailing edge of Read Stobe until interface device bus drivers are in Tri-State mode	0		250	ns	

Table 5. Timing: Data from Microprocessor to Peripheral

Symbol	Parameter	Min.	Typ.	Max.	Units	Comm.
t_{ACS0}	Address Bus Valid to Chip Select ON (CS = 0)		40		ns	$V_{DD} = 5V$
t_{CSW}	Chip Select ON to Write Probe	310	450		ns	
t_{AW}	Address Bus Valid to Write Strobe	350			ns	
t_{WW}	Write Strobe Width	430			ns	
t_{DW}	Data Bus Valid before Write Stobe	50			ns	
t_{WD}	Address Bus hold time following Write Strobe	100			ns	
t_{WA}	Data Bus hold time following Write Strobe	50			ns	
t_{ACS1}	Address change to Chip Select OFF (CS = 1)		40		ns	